Hall Ticket Number:

Code No. : 15444 S N/O

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS), HYDERABAD
Accredited by NAAC with A++ Grade
B.E. (E.C.E.) V-Semester Supplementary Examinations, June-2023
Integrated Circuits and Applications

Time: **3 hours**

Max. Marks: **60**

*Note: Answer all questions from **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

Q. No.	Stem of the question	M	L	CO	PO
1.	Write the ideal characteristics of Op-Amp.	2	1	1	1
2.	Draw the transfer characteristics of comparator given below. Assume $+V_{sat} = -V_{sat}=15V$, $V_{ref}=5V$ and Op-amp is ideal.	2	2	2	1
3.	State the advantages and disadvantages of Active filters.	2	1	2	1
4.	A mono stable multivibrator is designed using 555 timer. Determine the value of resistance required for output pulse with of 1.1ms. Assume $C=0.1\mu F$.	2	2	3	2
5.	List features of IC723 voltage regulator.	2	1	3	1
6.	Determine the resolution of 8-bit ADC for full scale input voltage of 10mv.	2	2	3	2
7.	Define figure of merit and noise margin of a logic gate.	2	1	4	1
8.	Determine fanout of a logic gate for $I_{OH}=1mA$, $I_{OL}=10mA$, $I_{IH}=1\mu A$ and $I_{IL}=1mA$.	2	2	4	2
9.	Draw the circuit diagram of 3-bit adder using IC7483.	2	2	5	1
10.	What are the applications of a shift register?	2	2	5	1

Part-B (5×8 = 40 Marks)

11. a)	Design a closed loop inverting amplifier using Op-Amp for a gain of 10 and input impedance of 10KΩ.	4	3	1	3,PSO1
b)	Explain the working of sample and hold circuit using Op-amp with the help of neat circuit diagram.	4	2	2	2

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			M	L	CO	PO
12.	a)	Design a second order low pass Butterworth filter for cutoff of frequency of 1KHz .Assume C=1µF.	4	3	2	3, PSO1
	b)	Explain the operation of Astable multivibrator using 555 timer.	4	1	3	2
13.	a)	Design a voltage regulator using IC723 for an output of 5V and maximum load current of 25mA.	4	3	3	3, PSO1
	b)	Describe the working of dual slope ADC with the help of neat circuit diagram.	4	2	3	2
14.	a)	Draw the diagram of 2-input standard TTL NAND gate and explain its working.	4	2	4	2
	b)	Compare TTL logic family with CMOS logic family.	4	3	4	2
15.	a)	Design a 8-bit magnitude comparator using IC 7485.	4	3	5	3
	b)	Design a Mod-8 counter using IC7490.	4	3	5	3, PSO1
16.	a)	Design a lossy integrator using Op-Amp for an input signal frequency of 1KHz and pass band gain of 2.	4	3	1	3
	b)	Draw the block diagram of IC 8038 function generator and describe its working.	4	2	3	2
17.		Answer any *two* of the following:				
	a)	Explain the operation of inverted R-2R Ladder type DAC with an example.	4	2	2	2
	b)	Draw the circuit diagram of tri-state TTL NOT gate and explain its working.	4	1	4	2, PSO1
	c)	Design a pseudo random sequence generator using 4-bit shift register (IC7495).	4	3	5	3

M : Marks;   L: Bloom's Taxonomy Level;   CO; Course Outcome;   PO: Programme Outcome

i)	Blooms Taxonomy Level – 1	20%
ii)	Blooms Taxonomy Level – 2	40%
iii)	Blooms Taxonomy Level – 3 & 4	40%

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